High Speed Switch/Router Design

By Jian-Guo Chen

Date: October 18, 2001 (Thursday)
Time: 5:00 pm (refreshment starts at 4:45pm)
Place: 204 Kupfrian Hall, NJIT

About the Speaker

Jian-Guo Chen is a member of technical staff in the Network Processor and Switch (NPS) group of Agere Systems Inc. At Agere, he is responsible for architecture design of IP routers/network processors, especially traffic management part. Currently, he is working on the 10G network processor architecture design. Before joining Agere, he worked at Bell Labs of Lucent Technologies on the ATM switch design since January 1997. Dr. Chen received his Ph. D. degree in electrical engineering from the New Jersey Institute of Technology, Newark, in 1997.

About the Talk

This talk will focus on various aspects of implementing high speed switches/routers. It will cover such operations as: table lookup/classification, traffic policing, buffer management, traffic buffering, queuing, and scheduling. This talk will also cover the issues switch/router designers have to face when the networking speed scales up from OC-48 to OC-192 and beyond, especially the memory bandwidth and latency related issues.

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