NJIT New Jersey's Science & Technology University

IEEE North Jersey Communications Chapter

Architectural Supports to Resolve Physical Problems (Power, Temperature, and Soft error)

by Prof. Sung Woo Chung,
Computer and Communication Engineering, Korea University, Seoul, Korea

Date: February 22, 2007 (Thursday)
Time: 4:00 pm (refreshment starts at 3:45 pm)
Place: 202 ECEC, NJIT

About the Speaker

Dr. Sung Woo Chung received his B.S. in Computer Engineering from Seoul National University, Seoul, Korea in 1996, and his Ph.D. in Electrical and Computer Engineering from Seoul National University in 2003. During his Ph.D. courses, he worked for IBM T.J. Watson Research Center, Yorktown Heights, USA as an intern for six months. After graduation, he had worked for Samsung Electronics as a senior engineer for 2.2 years, where he architecturally improved ARM1136 and AXI (AMBA 3.0) for Samsung's SoC (System on Chip). In 2005, he worked as a research scientist in University of Virginia, Charlottesville, USA. From 2006, he is an assistant professor in Computer and Communication Engineering of Korea University, Seoul, Korea.

About the Talk

As process technology scales down, process/circuit techniques are not enough to resolve physical problems – power, temperature, and soft error. In this talk, I would like to present some of my recent architectural contributions to these issues. 1) Power: Leakage power in instruction caches is reduced by the drowsy cache concept and the proposed new wakeup prediction policy that utilizes branch prediction information. The key insight is that branch prediction can be used to selectively wake up only the needed cache line. 2) Temperature: a) The number of CMOS sensors is limited due to the design budget. The “soft” thermal sensor that is based on the activity and simple regression can augment CMOS sensors. b) To evaluate OS-level scheduling policies in Linux, a new thermal simulation environment was proposed, which will be explained. c) A thermal virus can potentially incur malfunctions and eventually hardware failure. Its possibility and solution will be presented. 3) Soft Error: Regarding the soft errors in the instruction cache. Soft errors in the instruction caches are shown to be changed into refetching with negligible performance degradation. On the soft errors in the logic, idle pipeline paths can be used for fault-tolerance with dissipating only small amount of power.

Sponsors: **IEEE Communications Society North Jersey Chapter**
NJIT Department of Electrical and Computer Engineering

For more information contact Jie Hu (973) 596-5273/Nirwan Ansari (973) 596-3670 or check **http://web.njit.edu/~ieeenj/comm.html** for latest updates. Directions to NJIT can be found at: **http://www.njit.edu/University/Directions.html**.