Reliability of Thin Oxides Grown on Deuterium Implanted Silicon Substrate

D. Misra and R. K. Jarwal

***Abstract*—We have investigated the reliability of gate oxide with deuterium incorporated at the Si/SiO$_2$ interface through low energy ion implantation into the silicon substrate before thin gate oxide growth. Deuterium implantation at a dose of 1×10^{14}/cm^2 at 25 keV showed improved breakdown characteristics. Charge-to-breakdown seems to correlate well with the interface state density measured by conductance method.**

I. INTRODUCTION

Interest in incorporation of deuterium at the Si/SiO$_2$ interface for hot-carrier lifetime improvement in CMOS devices has increased in recent years [1]–[3]. Significant portion of the dangling bonds at the Si/SiO$_2$ interface is satisfied by deuterium. Typically, many hours of annealing is used for deuterium incorporation [4]. In some cases, high-pressure deuterium annealing is used to reduce annealing time [5]. Recently, extended annealing time and temperature at a higher deuterium concentration was overcome by deuterium implantation before gate oxide growth [6]. Deuterium implantation is suitable for integrated circuits with multilevel dielectric or metallization layers or where Si$_x$N$_y$ is used as a sidewall spacer as Si$_x$N$_y$ could form a diffusion barrier for deuterium [7]. The reliability of the gate oxide that is grown on a deuterium implanted silicon substrate must be determined before this process can be used in integrated circuit processing. This work reports the breakdown characteristics of silicon dioxide when deuterium is incorporated at the Si/SiO$_2$ interface through low energy ion implantation into silicon substrates before thin gate oxide growth. Oxides grown without any deuterium implantation were used as control devices.

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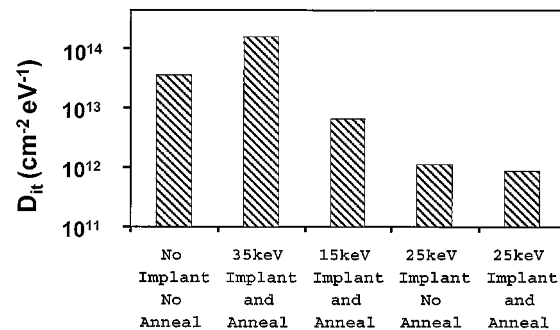

Fig. 1. Peak $D_{\rm it}$ values measured by conductance method at 1 MHz as a function of gate voltage for various devices.

II. EXPERIMENTAL

Deuterium was implanted at room temperature (300 K) into (100) p-type Si substrates with a resistivity of 1.25–2.0 Ω-cm at 15, 25, and 35 keV with a dose of 1×10^{14}/cm^2 through a 200 Å sacrificial oxide. The sacrificial oxide was used to avoid any irreparable surface damage. SRIM simulations for the above energies resulted in peaks at 0.38 μm, 0.6 μm, and 0.75 μm, respectively. After the sacrificial oxide was etched, the gate oxide was grown in dry O$_2$ at 800 °C for 20 min. The oxide thickness was 40 Å for all the splits. The gate oxide thickness was measured by ellipsometry on 16 sites of each Si wafer to obtain an average value. Deuterium implantation did not cause any apparent thickness variation within a wafer or across the wafers. Some of the wafers were annealed at 850 °C for 20 min in N$_2$O ambient. A 3000 Å polycrystalline silicon layer was then deposited at 600 °C and patterned using reactive ion etching to form MOS capacitors with 50 μm diameters. Conductance method at 1 MHz was employed by using a HP 4156B parameter analyzer to estimate interface state density ($D_{\rm it}$). Charge-to-breakdown measurement was performed by gate injection mode at a constant current of 400 mA/cm^2.

III. RESULTS AND DISCUSSION

Fig. 1 shows the peak interface state density values measured by the conductance method. $D_{\rm it}$ is much smaller for the 25 keV-implanted oxide compared to the nonimplanted oxide. Note that $D_{\rm it}$ for 15 keV-implanted and annealed devices is higher than that of the unannealed 25 keV-implanted devices. The 35 keV-implanted and annealed devices have larger $D_{\rm it}$ than the control devices. Annealed 25 keV-implanted devices show the lowest density of interface states. Implanted deuterium likely results in formation of Si-D bonding at the interface, which plays an important role in the change of distribution of deuterium in silicon during oxide growth and subsequent annealing. Once oxide is formed, the thermal energy to break the bond to silicon at the interface is higher than bulk silicon [8]. During thermal oxidation, deuterium diffuses either to the bulk or to the surface. Since the oxidation temperature (800 °C) is identical for all cases, interface passivation thus depends on the implantation conditions, as shown in Fig. 2. We speculate that for the 15 keV-implanted devices the increase in $D_{\rm it}$ indicates an absence of deuterium at the interface. The thermal budget used in this work contributed to outdiffusion of deuterium during oxidation for the 15 keV implanted devices. For the 25 keV-implanted devices, on the other hand, retention of deuterium was noticed after oxide growth when investigated by secondary ion mass spectroscopy (SIMS), reported elsewhere [9].

A reduction in $D_{\rm it}$ improves the charge to breakdown characteristics of the gate oxide [10]. The charge to breakdown for deuterium-im-

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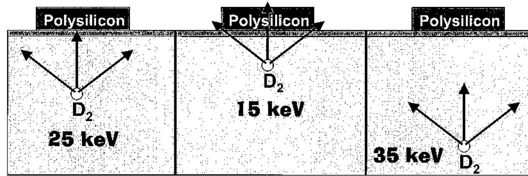

Fig. 2. Schematic representation of possible deuterium diffusion in silicon.

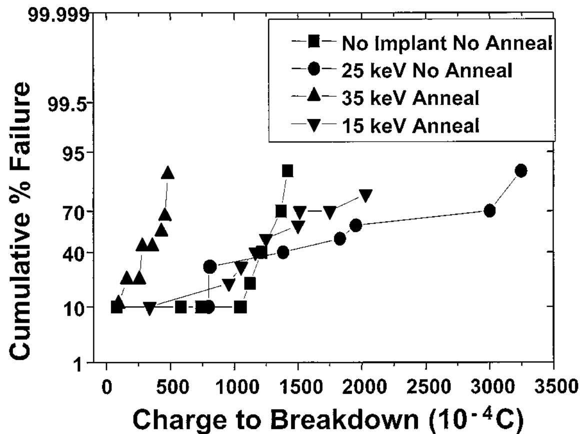

Fig. 3. Charge-to-breakdown characteristics for various devices measured by gate injection mode at a constant current of 400 mA/cm^2.

planted devices at different implantation energies is shown in Fig. 3. The 25 keV-implanted devices have the largest charge to breakdown characteristics. The 15 keV-implanted devices have a similar distribution of that of control devices. The 35 keV implanted devices have the worst charge to breakdown performance suggesting absence of deuterium at the interface. One possible explanation is that during oxidation (thermal budget), deuterium might have diffused into vacancies rather than diffusing toward the interface as the implantation depth ($\sim$0.75 μm) was rather deep for the 35 keV-implanted devices (Fig. 2). In addition, irreparable crystal damage is possible as the implantation energy is higher.

During electron injection, electron trapping establishes a high internal field in the oxide, which leads to increased hole current due to enhanced impact ionization [11]. The hole fluency leads to generation of new traps which also increases the electron trapping. Presence of deuterium at the interface suppresses the hole induced increase in the density of electron traps at the near interface region thereby increasing the charge to breakdown for the 25 keV-implanted devices. For all the devices, charge to breakdown behavior correlates well with that of interface state density. This result also confirms the dependency of charge to breakdown on interface states. It is known that the silicon-dangling bonds at the interface are the major contributors to the interface states density. The number of dangling bonds does not scale significantly with reduction in oxide thickness. Even though an oxide thickness of 40 Å is used in our work, deuterium incorporation using ion implantation can be achieved for thinner oxides.

IV. Conclusions

In summary, we have demonstrated that incorporation of deuterium at the silicon-silicon dioxide interface using ion implantation before the growth of gate oxide is an effective way of improving the oxide quality and reliability. This process may be a viable alternative to extended annealing through a "backend" process. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the charge to breakdown characteristics through reduction of interface states. Finally, the selection of appropriate implantation energy, implantation doses and annealing conditions can further optimize thin oxide quality.

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