Gate Oxides Grown on Deuterium-Implanted Silicon Substrate

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Thin oxides (4 nm) grown on deuterium-implanted silicon substrates were investigated for the first time. It was observed that deuterium implantation at a light dose of 1×10^{14}/cm^2 at 25 keV significantly reduced the leakage current through the oxide. A reduction in electron trap density has also been observed for this oxide. An increase in leakage current, observed for both higher and lower energy deuterium implants, was possibly because of enhanced substrate damage and out-diffusion of deuterium, respectively. Deuterium-implanted oxide, subjected to N$_2$O annealing, showed further improvement in electrical characteristics.
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Postmetal anneals in hydrogen ambient at low temperatures are used in metal oxide semiconductor (MOS) fabrication processes to passivate the silicon dangling bonds at the Si/SiO$_2$ interface.[1,2] This process step is required from a complementary MOS (CMOS) operation and circuit stability viewpoint since silicon dangling bonds lead to nonideal device characteristics and reduced channel conductance. However, MOS transistor performance can degrade as a result of desorption of hydrogen due to channel hot carriers. With ongoing miniaturization (scaling) efforts and complexity in device processing, the hot carrier reliability concerns are further exacerbated. In addition, latent damage in thin gate oxides due to plasma charging, a high-energy electron injection process, also causes significant reliability concerns as the hot carrier degradation is directly related to plasma charging damage.[3] Recently, an improvement was observed by a postmetallization annealing in deuterium ambient, instead of forming gas (hydrogen) at low temperatures (400–450°C).[4-6] Studies also indicate that transistors annealed in deuterium are much more resilient against plasma process induced damage[7] (as quantified by Si/SiO$_2$ interface trap generation and gate oxide leakage). Furthermore, stability of deuterated Si/SiO$_2$ interface has been found to improve with the isotopic substitution against degradation due to light and field exposure.[8] Therefore, there is a strong motivation to introduce deuterium at the Si/SiO$_2$ interface in CMOS manufacturing.

Though postmetal anneals in deuterium ambient can improve the interface quality,[4] it is necessary to anneal the wafers in deuterium ambient for hours to see any significant results in integrated circuits with multilevel dielectric/metallization layers. Since most CMOS processes require a minimum of three levels of the dielectric/metal interconnect process, the shadowing effect of multilevel metallization can make it really difficult for deuterium to reach the gate oxide/silicon interface. Besides, undoped polysilicon[9] and Si$_x$N$_y$, which is used as a sidewall spacer, could form a barrier for deuterium[5] during annealing. In this work, we report the electrical characteristics of silicon dioxide when deuterium was incorporated at the Si/SiO$_2$ interface by implanting it on silicon substrate before the thin gate oxide was grown. Different implantation energies were used. Implantation energy at 25 keV with a dose of 1×10^{14}/cm^2 was found to be most appropriate for device application. An N$_2$O anneal was performed to further improve the reliability characteristics and separate the effect of nitrogen and deuterium incorporation at the Si/SiO$_2$ interface. Oxides grown without any deuterium implantation and without any annealing were used as a reference device (control).

Experimental

If not chosen appropriately, implantation energy can cause significant substrate damage and thereby deteriorate oxide integrity. In addition, consumption of silicon during oxide growth and diffusion of deuterium must be taken into account to determine the appropriate implantation depth. Deuterium was implanted into (100) p-type Si substrates with a resistivity of 1.25-2.0 Ω cm at 15, 25, and 35
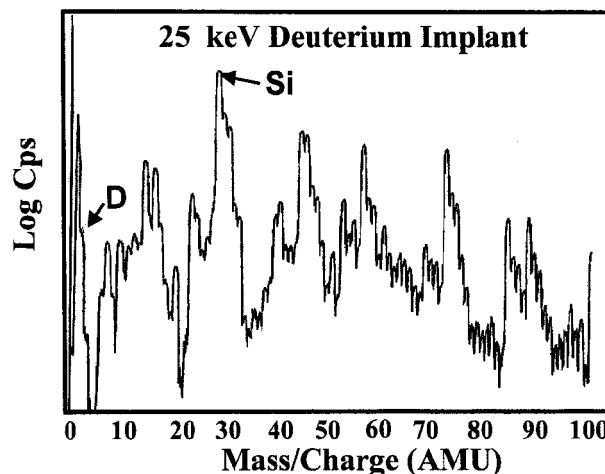

Figure 1. SIMS spectrum of 25 keV implanted sample after the growth of 40 Å of gate oxide at 850°C showing the presence of deuterium. Log *C*ps is logarithm (base 10) of counts per second and AMU is atomic mass units where oxygen is defined as 16.000.

keV with a dose of 1×10^{14}/cm^2 through a 200 Å sacrificial oxide.

SRIM simulations for the above energies resulted in peaks at 0.38, 0.6, and 0.75 μm, respectively. After the sacrificial oxide was etched, the gate oxide was grown in dry O$_2$ at 800°C for 20 min. The oxide thickness was 40 Å for all the splits. The gate oxide thickness was measured by ellipsometry on 16 sites of each Si wafer to obtain an averaged value. No apparent thickness variation was noticed due to deuterium implantation. An N$_2$O anneal was given at 850°C to some of the wafers. A 3000 Å polysilicon layer was then deposited at 600°C and patterned using plasma etching to form MOS capacitors with different diameters.

Results and Discussion

Figure 1 shows a secondary ion mass spectroscopy (SIMS) spectrum of the 25 keV implanted sample after the growth of the 40 Å of gate oxide. The spectrum was obtained using an incident ion energy of 4 keV Ar$^+$ with an O$_2$ background and it was integrated over the outer surface to several thousand angstroms deep. The distribution of deuterium within the sample cannot be determined by this spectrum since it does not provide any depth-resolved information. However, the presence of deuterium is noticed even though the wafer has gone through a high temperature oxide growth step.

Figure 2 shows the leakage current *vs.* gate voltage for the devices with and without deuterium implantation. The abrupt jumps in the curves are indicative of defect enhanced soft breakdown. Deuterium implanted at 25 keV devices showed the lower leakage current and breakdown characteristics compared to devices without any deuterium implant. The improvement in leakage current was observed, as a significant portion of the dangling bonds at the

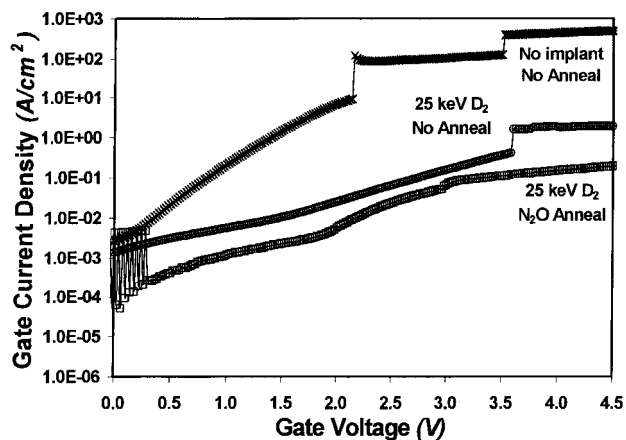* Electrochemical Society Active Member.
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Figure 2. Leakage current *vs.* gate voltage for the devices without and with 25 keV deuterium implantation. Data from samples with 25 keV deuterium implantation and N_2O annealing are also included.

Figure 3. I-V characteristics of devices with different deuterium implantation energies.

Figure 4. I-V characteristics of the MOS capacitors show the effect of deuterium implantation and subsequent N_2O annealing.

Si/SiO_2 interface were possibly passivated by deuterium. Note that deuterium passivated the dangling bonds like hydrogen at the interface since the chemistry of deuterium and hydrogen is virtually identical and either atom is equally suitable for passivating the dangling bonds at the interface. In this experiment, no forming gas anneal was used. The presence of deuterium, therefore, retards the charged defect sites at the interface, which reduces the leakage current through the oxide. When the deuterium-implanted sample was given an N_2O anneal, the characteristics improved further.

Figure 3 shows the current-voltage (I-V) characteristics of deuterium-implanted devices as a function of implantation energy. Though wafers implanted at 15 and 25 keV have comparable gate current densities, the 25 keV implanted wafer shows improved characteristics. This is possibly due to reduced retention of deuterium at the interface for the 15 keV implanted wafer. The implantation is quite shallow (0.38 μm) for 15 keV implantation, and therefore, during oxide growth it is possible for deuterium to diffuse out. The current density measured for 35 keV implantation is larger than even that for the control wafer, suggesting significant crystal damage occurred as the implantation energy was increased. The 25 keV implantation, on the other hand, shows the lowest leakage current in this experiment. This behavior indicates that proper control of implantation energy and dose during deuterium implantation can improve gate oxide reliability. Deuterium might diffuse out during oxidation if the implantation is too shallow as in low energy implants whereas high-energy implants can introduce substrate damage that is not repaired during the gate oxidation step.

Incorporation of nitrogen at the Si/SiO_2 interface through N_2O anneal, in addition to deuterium implantation further improves the oxide interface quality (Fig. 4). There is a clear reduction in leakage current with deuterium implantation and N_2O annealing. Reduction in leakage current was observed for control wafers (wafers without any implantation) when subjected to N_2O annealing. This suggests that the role of N_2 on the leakage current is different from that of deuterium, where nitrogen improves the interface stoichiometry by perhaps relieving strain or by replacing weak bonds at the Si/SiO_2 interface while deuterium satisfies the silicon dangling bonds. Both the effects reduce oxide interface trap concentration, which, in turn, reduces the leakage current.

The interface was exposed to a high field electron injection step during the patterning of polysilicon using plasma etching. To estimate the electron traps introduced during the above plasma-processing step, MOS capacitors were subjected to a constant current stress of 200 mA/cm^2 (gate injection). The slope of the initial portion of the voltage curve during injection represents the net electron-trapping rate, which is initially dominated by the filling of existing empty electron traps per injected electron under a particular stress
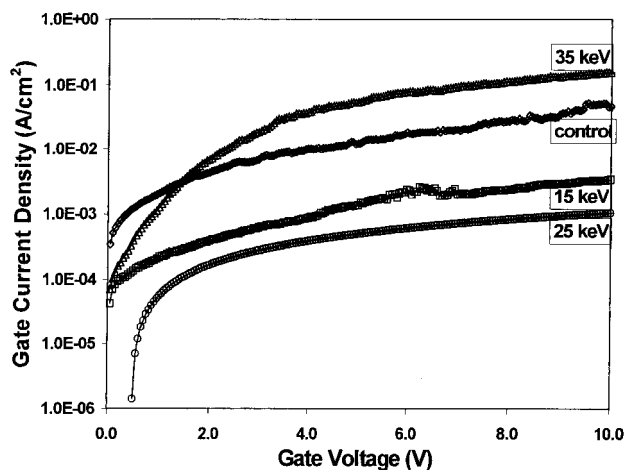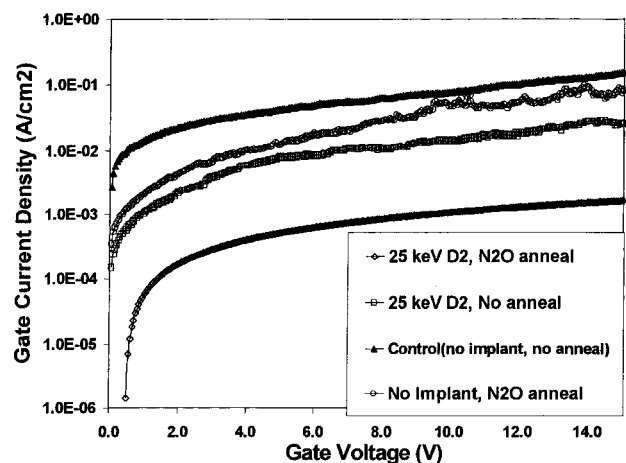
condition. The average values of the initial electron trapping slopes (IETS)[3] for all the devices are shown in Fig. 5. There is about an order of magnitude reduction over the control wafer in electron trap density with deuterium implantation and annealing. However, wafers with only deuterium implantation without any annealing also show improvement over the control sample. Under high field injection from the gate, electrons are first injected from the gate into the conduction band of SiO_2 owing to Fowler-Nordheim tunneling and gain kinetic energy from the oxide field. The electrons emitted into the substrate create electron-hole pairs, and the energy of the electrons is converted in part to electron-hole pairs. The mobile holes and/or released hydrogen/deuterium from the defect sites can move toward the gate interface where they create electron traps.[10] Implanted deuterium, therefore, led to passivation of the interface defect sites and contributed to the reduction of electron traps in the oxide since it is harder to release the D atom from the interface during electron injection. This was evident for deuterium-implanted samples which show lower IETS values. Finally, though N_2O annealing improved the oxide quality further, the deuterium-implanted device showed fewer electron traps compared to simple N_2O annealed samples (without implantation), justifying the above mechanism.

In summary, we have demonstrated that incorporation of deuterium at the silicon/silicon dioxide interface using ion implantation before gate oxide growth is an effective means to improve the oxide quality and may be a viable alternative to many hours of annealing
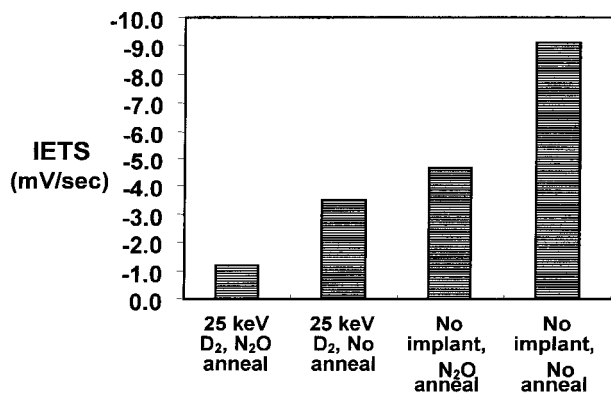
Figure 5. The average values of the initial electron trapping slope (IETS) for all the samples.

through a "backend" process. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the leakage current characteristics. Incorporation of nitrogen at the interface through N_2O annealing may further improve device performance because of improved interface stoichiometry. Reduction of electron traps is seen due to limited dissociation of implanted deuterium. It can be extrapolated that interfaces passivated through deuterium implantation can be less sensitive to hot electron stress. Finally, the selection of appropriate implantation energy, implantation doses, and annealing conditions are important for the optimization of thin oxide quality and reliability.

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