Plasma Damage Immunity of Thin Gate Oxide Grown on Very Lightly N$^+$ Implanted Silicon

K. P. Cheung, D. Misra, J. I. Colonell, C. T. Liu, Y. Ma, C. P. Chang, W. Y. C. Lai, R. Liu, and C. S. Pai

Abstract— **Plasma damage immunity of gate oxide grown on very low dose (2×10^{13}/cm^2) N$^+$ implanted silicon is found to be improved comparing to regular gate oxide of similar thickness. Both hole trapping and electron trapping are suppressed by the incorporation of nitrogen into the gate oxide. Hole trapping behavior was determined from the relationship between initial electron trapping slope (IETS) and threshold voltage shifts due to current stress. This method is believed to be far more reliable than the typical method of initial gate voltage lowering during current stress.**

I. Introduction

Very thin gate oxides are required for continue device scaling into the deep submicron regime. The reliability of these very thin gate oxides is naturally a very important concern. One of the stress modes that do not scale with the oxide thickness is plasma-charging damage. Improving the gate oxide's immunity to plasma-charging damage is therefore a high priority issue. There has been much work centering on the effect of incorporated nitrogen in improving gate oxide reliability [1]. A recently introduced method of incorporating nitrogen into the gate oxide is to implant N$^+$ into the substrate before gate oxide growth [2]. In this paper, we like to report a study of plasma damage immunity improvement using this method of nitrogen incorporation. In order to see how sensitive is the improvement on N$^+$ implant, we concentrate our present report on very light dose of $2 \times 10^{13}/\text{cm}^2$ case only. At this dose level, the gate oxide growth rate was not affected (within the 3% measurement uncertainty) by the nitrogen [2] and thus allows a very close comparison study.

II. Experimental

Wafers were processed to metal 1 using a 0.25 μm CMOS technology. The N$^+$ split was accomplished by introducing an additional blanket implant step. Otherwise, the control (thermal oxide) and split (N$^+$ oxide) are exactly the same and processed together through out. Gate oxide thickness was 52 Å for both types as measured by multi-angle ellipsometry and TEM. N$^+$ was implanted through a 200-Å sacrificial oxide using 25 keV energy. The sacrificial oxide was removed before gate oxide was grown (dry O_2 at 800 °C, 25 min). Wafers were anneal in forming gas (400 C, 30 min) before measurement.

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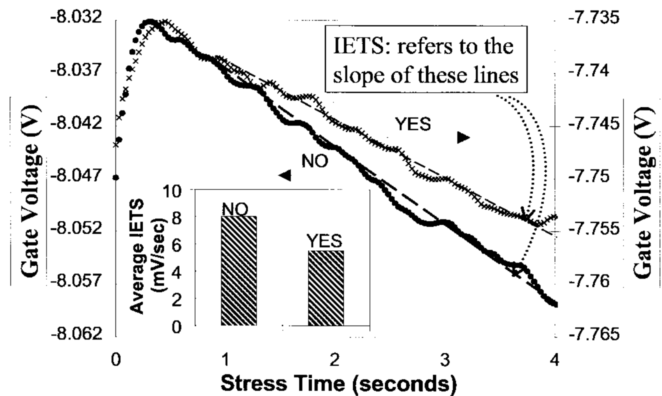

Fig. 1. V-T curves @ 400 mA/cm^2 constant current stress of oxides with (YES) and without (NO) low dose ($2 \times 10^{13}/\text{cm}^2$) N$^+$ implant. Insert shows the average initial electron-trapping slope (IETS) of 42 devices for each type of oxide.

N-channel transistors with antenna ratio of $2571:1$ were used in this study. Threshold voltage (V_t) and transconductance (G_m) before stress were very uniform across the wafer. Each transistor was subjected to a 400 mA/cm^2 constant current stress for 4.5 s using gate injection mode. Initial electron trapping slopes (IETS) [3] were extracted from the voltage curve during stress. Post stress transistor measurements were done at fixed delay of 10 s. V_t and G_m shifts (ΔV_t and ΔG_m) due to stress were obtained from subtracting the before stress values from the after stress values.

III. Results and Discussion

Fig. 1 shows the typical voltage curves for the two types of oxide. Both are dominated by hole trapping at first (gate voltage (V_g) become less negative) and then electron trapping takes over (hole trapping saturated). The noise in the curves is due to instrument (HP4145A). The electron trapping rate (IETS—slope of the dotted lines in Fig. 1) is clearly lower in the N$^+$ oxide, which implies lower electron trap density. The small difference in V_g is an indication of the N$^+$ oxide is actually thinner than nonimplanted oxide by about 3% (V_g is very sensitive to oxide thickness). The average IETS of 42 devices is shown in the insert. These wafers were processed in a known plasma-charging damage (the power-lift step at the end of PETEOS deposition [10]) tool during fabrication. The increase in IETS (the damage-free IETS is ~4 mV/s) for both oxides are indication of electron trap density increase due to charging damage. The increase is lower for the N$^+$ oxide.

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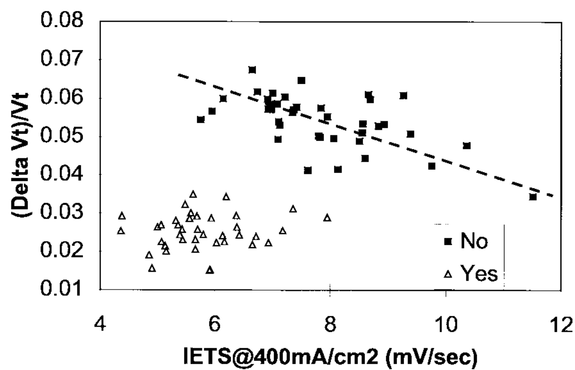

Fig. 2. $\Delta V_t/V_t$ due to current stress as a function IETS for both with (YES) and without (NO) N^+ implanted samples. $\Delta V_t/V_t$ for YES devices does not follow the same trend as NO devices.

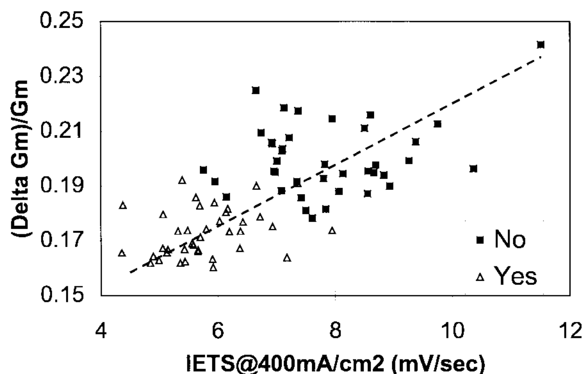

Fig. 3. $\Delta G_m/G_m$ due to current stress as a function of IETS for both with (YES) and without (NO) N^+ implanted substrates. The $\Delta G_m/G_m$ value for both oxides merge into the same trend.

Fig. 2 plots the $\Delta V_t/V_t$ versus IETS. For the devices with normal oxide, $\Delta V_t/V_t$ is linearly related to IETS with a negative slope as expected [3]. For a given oxide, hole trapping depends only on the level of current stress while electron trapping increases with damage. The net amount of positive charge (hence $\Delta V_t/V_t$) in the oxide therefore decreases with damage [3]. Note that once the IETS is fixed, the amount of trapped electrons is also fixed. If the N^+ oxide's hole trapping behavior is similar to normal oxide, they should follow the same trend. As can be seen from Fig. 2, devices with N^+ oxide have a low IETS and a low $\Delta V_t/V_t$ at the same time indicating a lower than expected density of trapped holes.

Most hole trapping studies rely on determining the amount of V_g lowering at the initial stage of the gate voltage curve. Arakawa *et al.* [4] found increasing nitrogen content in the gate oxide increases hole trapping. Yoon *et al.* found higher hole trapping in N_2O oxide than pure oxide during current stress [5]. Crook *et al.* [6], on the other hand, found no difference between N_2O oxide and pure oxide. We believe our result is more reliable for the following reason.

All the above studies suffered from the fact that starting V_g cannot be determined experimentally. The problem can be summarized as follow: The first step in current stress is to charge up the capacitance of the system. The V_g should rise rapidly at first and then turn around when the voltage change due to hole trapping is larger than due to capacitance charging. Most measurements (including this one) are unable to resolve this part of the curve. Clearly, the first point in the voltage curve is not the real starting V_g at all. Even with better time resolution, the early behavior of the V_g curve would depend on the capacitance of the system, the rate of hole trapping and the oxide thickness. The measured V_g lowering that commonly interpreted as hole trapping level thus is completely arbitrary. The degree of uncertainty is less but not eliminated when using the same measurement system to do qualitative comparison between different material types.

Fleetwood *et al.* [7] used a thermally stimulated-current (TSC) method to measure trapped holes and found that hole trapping depends strongly on the way nitrogen is introduced into the gate oxide. When done properly, nitrided oxide can have lower hole trapping level than thermal oxide. Our result agrees with their finding indicating that N^+ implant into silicon before gate oxide growth is a good way to introduce nitrogen into the gate oxide.

Unlike $\Delta V_t/V_t$, the $\Delta G_m/G_m$ behavior (Fig. 3) for both types of oxide follows the same trend as reported previously [3], increases with IETS. The $\Delta G_m/G_m$ for N^+ oxide is, as expected, lower than normal oxide after the same stress. As discussed in [3], IETS is completely insensitive to the trap states at the SiO_2/Si interface. Yet, IETS is linearly proportional the $\Delta G_m/G_m$, a quantity that is most sensitive to interface state density. Note that the forming gas anneal should passivate the interface states before stressing, and should normally wipe out the memory of damage. However, interface states generated by plasma damage may behave differently. It has been observed that damage induced interface states reappear more readily upon further stress [8]. If our observed $\Delta G_m/G_m$ is indeed dominated by damage-related interface states, then these damage-related interface states must linearly proportional to the damage generated bulk electron traps. From the detrapping kinetic study [9], we, however, tend to believe that our observed $\Delta G_m/G_m$ change is due to near interface electron traps. The suppressed G_m degradation thus serves as another evidence that electron trap generation in N^+ oxide is suppressed.

In conclusion, we found that even a very low dose of N^+ implant before gate oxide growth can improve gate oxide's resistance to plasma-charging damage. We found that both electron trapping and hole trapping are suppressed effectively.

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