Metal-oxide-silicon diodes on deuterium-implanted silicon substrate

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Ion implantation was used to incorporate deuterium at the $Si-SiO_2$ interface. Polycrystalline silicon gate metal-oxide-semiconductor diodes with 4 nm oxide grown on deuterium-implanted *p*-type $\langle 100 \rangle$ silicon substrate were investigated. It was observed that deuterium implantation at a light dose of $1\times10^{14}/cm^2$ at 25 keV reduced oxide leakage current due to reduction in oxide charge and interface traps. Low-energy implant indicates possible deuterium loss during oxidation whereas in case of higher energy implant, the observed degradation was caused by enhanced substrate damage. Interface state density D_{it} as obtained from the conductance measurements suggests that implanted deuterium passivates the interface traps. © *2000 American Institute of Physics.* [S0003-6951(00)04721-5]

Role of hydrogen in metal-oxide-semiconductor (MOS) device stability and reliability has long been known. It is believed that hydrogen passivates silicon-dangling bonds at the $Si-SiO_2$ interface[1,2] thereby reducing the interface trap density. But MOS transistor performance continued to degrade due to channel hot carriers as a result of desorption of hydrogen from the passivated sites. Lyding, Hess, and Kizilyalli[3,4] recently reported significant improvement in hot carrier lifetime when the interface was passivated by deuterium rather than usual hydrogen. This development inspired a new wave of interests in deuterium in the $Si-SiO_2$ system.[5–8] Mogul *et al.*[5] showed that deuterium sintered submicron devices are less prone to degradation due to electrical stress than forming gas annealed devices. Similarly, Devine *et al.*[6] confirmed that the degradation in channel transconductance is mainly due to creation of interface states and a significant reduction in interface states were noticed for deuterium annealed devices. In a complementary study, the characteristics of deuterium as a function of thermal annealing was examined in thin SiO_2 films[7] and in complementary-metal-oxide-semiconductor (CMOS) devices.[8]

While these results are encouraging, significant challenges still remain as far as the integration of deuterium annealing into mainstream semiconductor manufacturing are concerned. The noticeable improvement in hot carrier lifetime in deuterium annealed samples could be unstable and relaxed when the samples are subjected to further processing.[9] Second, when CMOS technologies incorporate multiple metal and dielectric layers, the improvement due to deuterium sintering was reduced further.[10] In addition, undoped polycrystalline silicon[8] and Si_xN_y, used as a sidewall spacer, could limit the transportation of deuterium to the $Si-SiO_2$ interface during annealing by serving as a diffusion barrier for deuterium.[10] In some processes, these limitations were overcome by extended time and temperature anneals at higher deuterium concentration[11] but cycle time associated with extended anneals and detrimental effects of higher temperatures on the long-term metal properties require exploring possible alternatives for deuterium incorporation at the $Si-SiO_2$ interface. In CMOS processing middle-of-line and back-end-of-line deuterium anneals were suggested.[12] In an alternative approach,[13] when gate oxide was grown in D_2O ambient, the interface state density was not only reduced the process also suppressed charge trapping in the oxide.[13] The characteristics of deuterium at the $Si-SiO_2$, therefore, is not very well understood.

In this work, we report the electrical characteristics of MOS diodes when deuterium was incorporated at the $Si-SiO_2$ interface by ion implantation into silicon substrate before the thin gate oxide was grown. This approach will streamline process integration and reduce cycle time. Ion implantation of deuterium in bare silicon and silicon oxide systems has been studied.[14] Park and Helms in the same study[14] while evaluating the effect of annealing on the distribution of deuterium, have shown that the release of deuterium from bare silicon is possible at 600 °C whereas deuterium could diffuse out completely from $Si-SiO_2$ system at 900 °C. It will be, therefore, important to investigate oxide/interface quality when the oxide was grown on deuterium-implanted silicon substrate. Besides, ion implantation conditions can be sensitive to experimental outcome. If not selected appropriately, implantation energy can cause irreparable substrate damage and thereby deteriorate oxide integrity. Though different implantation energies were used, implantation energy of 25 keV with a dose of $1\times10^{14}/cm^2$ was found to be most appropriate for device applications. Oxides grown without any deuterium implantation and without any annealing were used as a reference device (control).

Deuterium was implanted at room temperature (300 K) into (100) *p*-type Si substrates with a resistivity of 1.25–2.0 Ω cm at 15, 25, and 35 keV with a dose of $1\times10^{14}/cm^2$ through a 200 Å sacrificial oxide. The sacrificial oxide was used to avoid any irreparable surface damage. SRIM simulations for the above energies resulted in peaks at 0.38, 0.6, and 0.75 μm, respectively. After the sacrificial oxide was etched, the gate oxide was grown in dry O_2 at 800 °C for 20 min. The oxide thickness was 40 Å for all the splits. The gate

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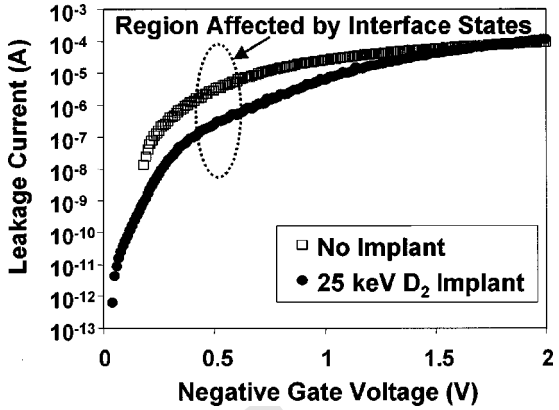

FIG. 1. Leakage current vs negative gate voltage measured on *p*-type ⟨100⟩ MOS device with 4 nm gate oxide.

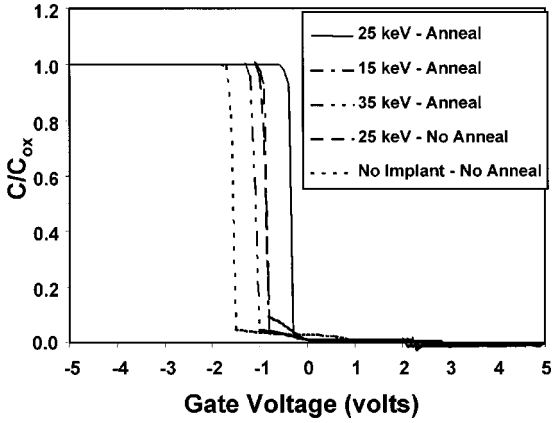

FIG. 2. Measured normalized high-frequency capacitance and voltage characteristics of deuterium implanted devices.

oxide thickness was measured by ellipsometry on 16 sites of each Si wafer to obtain an averaged value. No apparent thickness variation was noticed due to deuterium implantation. Some of the wafers were annealed at 850 °C for 20 min in N_2O ambient. A 3000 Å polycrystalline silicon layer was then deposited at 600 °C and patterned using reactive ion etching to form MOS capacitors with 50 μm diameters. The devices were characterized using current voltage ($I-V$) and high frequency $C-V$ measurements. Conductance method at 1 MHz was employed by using an HP 4156B parameter analyzer to estimate interface state density (D_{it}).

Figure 1 shows typical $I-V$ characteristics for the devices with and without deuterium implantation. The $I-V$ measurement shows an overall decrease in leakage current for 25 keV deuterium-implanted device compared to device without any deuterium implant. As the negative gate voltage increases above ~0.3 V the silicon surface moves through the flat band condition where interface states, which act as charge storage centers, increase the current through the oxide.[15,16] Gate voltage above the flat band voltage V_{fb} (~1.1 V) conduction is mainly due to Fowler–Nordheim (FN) tunneling, therefore, both the devices show similar behavior. The observed improvement in leakage current for the deuterium implanted device was possibly due to passivation of interface states at the Si–SiO_2 interface by deuterium. Deuterium passivates the dangling bonds like hydrogen at the interface since the chemistry of deuterium and hydrogen is virtually identical and either atom is equally suitable for passivating the dangling bonds at the interface. Note that, in this experiment no forming gas anneal was used. The presence of deuterium therefore retards the charged defect sites at the interface, which reduces the leakage current through the oxide.

The high frequency $C-V$ curves reveal that deuterium implantation induces a positive gate voltage shift as shown in Fig. 2. It is known that $C-V$ curves are affected by the capacitive response of fast interface states. Notice that deuterium implanted at 25 keV devices showed increased interface passivation of the dangling bonds at the Si–SiO_2 interface compared to devices without any deuterium implant. For the annealed 25 keV deuterium-implanted sample the measured curve suggests significantly reduced interface states and oxide charge. It is known that postoxidation annealing reduces oxide charge. Wafers implanted at 25 keV (no anneal) have comparable $C-V$ profile with that of 15 keV implanted and annealed devices. The effect of annealing might have improved the $C-V$ characteristics of 15 keV implanted and annealed devices. This is possibly due to reduced retention of deuterium at the interface for the 15 keV implanted (annealed) wafer. The implantation is rather shallow (0.38 μm) for 15 keV implantation and therefore during oxide growth outdiffusion of deuterium is possible. The $C-V$ curve measured for 35 keV implantation and annealed sample is not much better than the control wafer, suggesting irreparable crystal damage occurred as the implantation energy was increased. In addition, since the implantation depth for 35 keV implantation is rather deep (approximately 0.75 μm), during oxidation deuterium might have diffused into vacancies rather than diffusing towards the interface. Retention of deuterium in the 25 keV implanted sample after the growth of the 40 Å of gate oxide was noticed when investigated by secondary ion mass spectroscopy (SIMS) and reported elsewhere.[17] The observed behavior in $C-V$ characteristics, therefore, indicates that proper control of implantation energy and dose during deuterium implantation can improve gate oxide and interface reliability.

To confirm the assumptions from $I-V$ and $C-V$ measurements, conductance method was employed to measure the interface trap density D_{it}. Figure 3(a) shows measured conductance at 1 MHz as a function of gate voltage. The magnitude of the conductance peak is much smaller for the 25 keV implanted oxide compared to no implant oxide. The comparable conductance peak for 15 keV deuterium implantation shows some improvements over the control device but much higher than that of the 25 keV implanted devices.

The peak D_{it} values for various deuterium-implanted devices are shown in Fig. 3(b). We determine that the initial density of interface states (no implant and no anneal) is rather high with a peak value around $10^{13}\,cm^{-2}\,eV^{-1}$. As can be seen in Fig. 3(b) D_{it} decreases with deuterium implanted samples. The 25 keV deuterium implanted and annealed sample shows the lowest density of interface states. Even though annealing reduces D_{it}, notice that D_{it} for 15 keV implanted and annealed sample is higher than that of the unannealed 25 keV implanted device. This agrees well with our findings from the $C-V$ measurement that some of the deuterium is lost during oxide growth due to outdiffusion. In

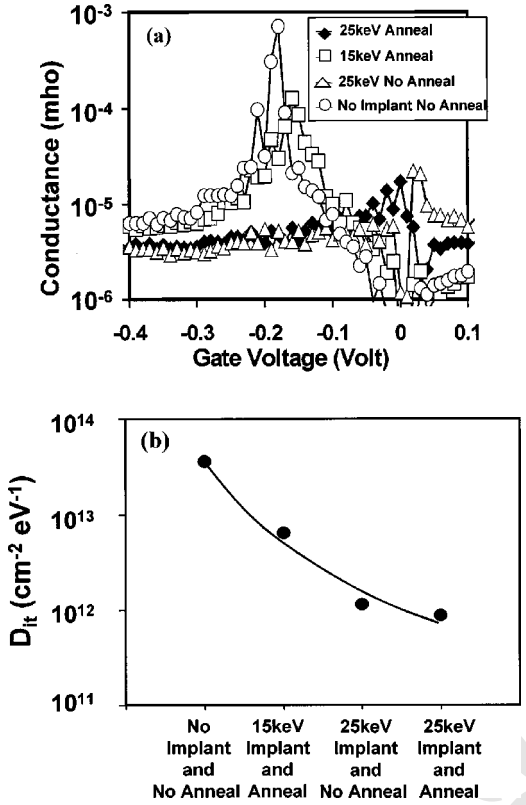

FIG. 3. Measured conductance at 1 MHz as a function of gate voltage for various samples (a) and the peak D_{it} values are depicted in (b).

addition, the improvement in D_{it} for 25 keV implanted and annealed sample indicate a completely different behavior of deuterium if oxide is grown on the implanted substrate compared to annealing of bare silicon.[14] It seems that if the implantation dose is appropriate, deuterium tends to remain at the interface during oxide growth. However, if the implantation dose is high ($\sim$35 keV implant)[17] the thermal budget may not be able to remove the implantation damage.

The variation of interface-state densities versus energy with respect to midgap are shown in Fig. 4 for deuterium implanted samples. We only compared the 25 keV deuterium implanted (annealed and unannealed) with that of no implant and no anneal sampled. The interface states were sensitive to $\sim$1 μs and the slower states were not investigated in this experiment. It is clearly seen that interface states above the midgap are passivated for unannealed deuterium-implanted samples. It is interesting to note that the interface state density above the midgap has increased for the deuterium-implanted and 850 °C-annealed samples. However, it has the lowest D_{it} below midgap and above the valence band edge.

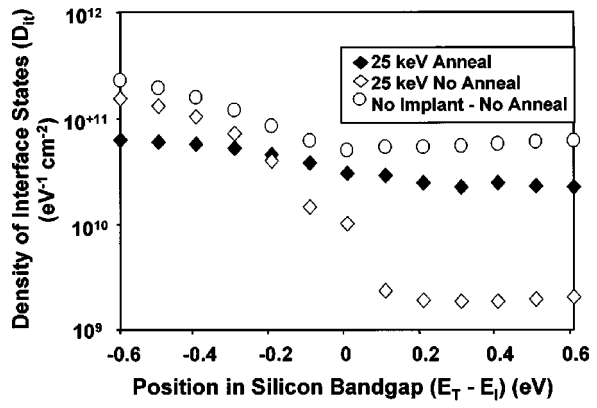

FIG. 4. Density of interface traps D_{it} as obtained from the conductance measurements. The trap energy E_T is with respect to intrinsic fermi level E_I.

Implanted deuterium likely results in formation of Si–D bonding,[18] which plays an important role in the change of distribution of deuterium in silicon during oxide growth and subsequent annealing. During oxidation deuterium diffuses either to the bulk or to the surface. Since the oxidation temperature (800 °C) is the same for all cases, contribution of deuterium to passivate the interface depends on the implantation condition. Once the oxide is formed the thermal energy to break the bond to silicon is higher than bare silicon system.[14] In addition, since deuterium is tied up with the silicon dangling bonds in large numbers at the interface the kinetics of breaking the Si–D bond at the interface is quite different from that of bulk silicon. Park and Helms[14] found that the release of deuterium from implantation induced Si–D or Si–OD configuration in Si–SiO_2 system occurs at around 900 °C. We believe, for 25 keV implanted sample the implantation depth and thermal budget retain most of the deuterium at the Si–SiO_2 interface.

The results of the present investigation of ion implantation of deuterium to passivate the silicon-dangling bonds indicate that the interface state density D_{it} is in accordance with the predicted behavior of P_b centers. It is known that P_b centers, though not the sole source, are the major contributors to D_{it}. In the (100) Si–SiO_2 interface, contribution of P_b centers to D_{it} is through the significant +/0 and 0/− levels at approximately $E_v+0.2$ eV and $E_v+0.85$ eV.[19] The D_{it} distribution in Fig. 4 for unannealed deuterium-implanted sample with the energy position about 0.2 eV above midgap shows significant reduction in D_{it} and corresponds well with EPR measurement for P_b center 0/− transition level of $E_v+0.85$ eV. Devine *et al.*[6] also found a peak around 0.2 eV above midgap for deuterium annealed interfaces. The characteristics of interface states in the deuterium-implanted devices, therefore, suggests that deuterium implantation contributes to the passivation of the P_b centers.

In summary, we have demonstrated that incorporation of deuterium at the silicon–silicon dioxide interface using ion implantation before gate oxide growth is an effective means to improve the oxide quality and may be a viable alternative to many hours of annealing through a middle-of-line or back-end process. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the oxide leakage current and capacitance–voltage characteristics. Reduction in preexisting bulk electron trap density has also been observed. A reduction in density of interface traps D_{it} as obtained from the conductance measurements for the deuterium-implanted devices suggests that deuterium implantation contributes to the passivation of the P_b centers. Finally, the selection of appropriate implantation energy, implantation doses, and annealing conditions are important for the optimization of thin oxide quality and reliability.

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[1] P. Balk, The Electrochemical Society Extended Abstracts, San Francisco, CA, May 9–13, 1965, Abstract 109, p. 237, Vol. 65-1.
[2] N. M. Johnson, D. K. Biegelsen, and M. D. Moyer, J. Vac. Sci. Technol. **19**, 390 (1981).
[3] J. W. Lyding, K. Hess, and I. C. Kizilyalli, Appl. Phys. Lett. **68**, 2526 (1996).
[4] K. Hess, I. C. Kizilyalli, and J. W. Lyding, IEEE Trans. Electron Devices **45**, 406 (1998).
[5] H. C. Mogul, L. Cong, R. M. Wallace, P. J. Chen, T. A. Rost, and K. Harvey, Appl. Phys. Lett. **72**, 1721 (1998).
[6] R. A. B. Devine, J.-L. Autran, W. L. Warren, K. L. Vanheusdan, and J.-C. Rostaing, Appl. Phys. Lett. **70**, 2999 (1997).
[7] I. J. R. Baumvol, E. P. Gusev, F. C. Stedile, F. L. Freire, M. L. Green, and D. Brasen, Appl. Phys. Lett. **72**, 450 (1998).
[8] P. J. Chen and R. M. Wallace, Appl. Phys. Lett. **73**, 3441 (1998).
[9] W. F. Clark, T. G. Ference, T. B. Hook, K. M. Watson, S. W. Mittl, and J. S. Burnham, IEEE Electron Device Lett. **20**, 48 (1999).
[10] J. Lee, Y. Epstein, A. C. Berti, J. Huber, K. Hess, and J. W. Lyding, IEEE Trans. Electron Devices **46**, 1812 (1999).
[11] I. C. Kizilyalli, G. Weber, Z. Chen, G. Abeln, M. Schonfield, B. Kotzias, F. Register, E. Harris, S. Sen, S. Chetlur, M. Patel, L. Stirling, R. Huang, A. Massengale, P. K. Roy, G. Higashi, E. Foley, J. Lee, J. Lyding, and K. Hess, IEEE IEDM Tech. Dig. 935 (1998).
[12] W. F. Clark, P. E. Cottrell, T. G. Ference, S.-H. Lo, J. G. Massey, S. W. Mittl, and J. H. Rankin, IEEE IEDM Tech. Dig. 89 (1999).
[13] H. Kim and H. Hwang, Appl. Phys. Lett. **74**, 709 (1999).
[14] H. Park and C. R. Helms, J. Electrochem. Soc. **139**, 2042 (1992).
[15] K. R. Farmer and R. A. Buhrman, Semicond. Sci. Technol. **4**, 1084 (1989).
[16] M. A. Green, F. D. King, and J. Shewchun, Solid-State Electron. **17**, 551 (1974).
[17] D. Misra and S. Kishore, Electrochem. Solid-State Lett. **2**, 637 (1999).
[18] E. H. Poindexter, Semicond. Sci. Technol. **4**, 961 (1989).
[19] G. J. Gerardi, E. H. Poindexter, P. J. Caplan, and N. M. Johnson, Appl. Phys. Lett. **49**, 348 (1986).