Plasma process-induced band-gap modifications of a strained SiGe heterostructure

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Exposure to plasma etching and subsequent annealing can relax the strain of coherently strained SiGe. This work investigates the change in valence-band discontinuity in plasma-exposed SiGe films due to strain relaxation by a capacitance–voltage ($C-V$) profiling technique using metal–oxide–semiconductor structures. Dry and wet etched samples annealed at 500, 600, 700, and 800 °C were investigated. Valence-band discontinuity ΔE_V at the Si/SiGe interface reduced with annealing temperature and completely disappeared at higher temperature annealing. Dry etched samples demonstrated a faster relaxation mechanism as compared to their wet etched counterparts. The $C-V$ method has turned out to be a simple, fast, and efficient approach to estimate any band-gap modifications in SiGe due to process-induced damage. © *1999 American Institute of Physics.* [S0003-6951(99)01921-X]

Reliability and electrical performance of strained Si/SiGe/Si heterostructure devices[1–4] may be significantly affected by plasma processing during device manufacturing.[5] Creation of strain-relieving misfit dislocation and/or threading dislocations may be possible when strained $Si_{1-x}Ge_x$ films are processed using reactive ion etching (RIE).[5] Though reactive ion etching of Si has been studied in detail,[6,7] not much is known about SiGe at present. In bulk semiconductors annealing causes condensation of point defects into dislocation loops which then shrink and disappear after further annealing. However, it is well known that SiGe samples thicker than the critical thickness, as per Matthews and Blakeslee,[8] annealed at temperatures higher than the growth temperature will have dislocation loops induced. The presence of such dislocation loops is known to relax the coherent strain of the SiGe layer. The strain relaxation mechanism for plasma etched samples annealed at temperatures lower than the growth temperature will be predominantly governed by the dislocation loops generated by plasma etching. On the other hand, for samples annealed above the growth temperature, the mechanism could be either due to plasma etching or due to the fact that the samples were annealed at a temperature higher than the growth temperature or both. Relaxation in strain (as a consequence of plasma etching and subsequent annealing) is expected to increase the band gap by reducing the valence-band discontinuity, and which eventually will reduce the carrier mobility in the fabricated device. Wet etching, on the other hand, is known to be a rather nondestructive method, and hence, retains the characteristics of the starting materials after the processing is done.

In this letter we have employed a capacitance–voltage ($C-V$) profiling technique to estimate the band gap of SiGe films exposed to plasma etching and subsequent annealing. Samples, with the cap layer partially removed by the plasma etch, were studied in this work. Wet etched samples were used for comparison. $C-V$ profiling is a fast and efficient approach to estimate plasma process-induced band-gap modifications since measurement techniques such as photoemission measurement, x-ray photoelectron spectroscopy, or photoreflectance measurement can be time consuming.

Typically, 15% of Ge is used to grow strained SiGe films for high-mobility advantages. Undoped 500-Å-thick $Si_{1-x}Ge_x$ ($x=0.15$) were grown on a p-Si ($2\times10^{16}\,cm^{-3}$) substrate by conventional chemical-vapor deposition (CVD) at 700 °C at atmospheric pressure. A 1500–1900-Å-thick Si cap layer was deposited on the $Si_{1-x}Ge_x$ layer. It should be noted here that the thickness of our SiGe sample (with 15% Ge) is more than the critical thickness as per Matthews and Blakeslee, which is 190 Å.[8] Plasma etching was performed in a DRYTECH 100 plasma reactor at a chamber pressure of 150 mTorr with a flow rate of 50 sccm SF_6 and freon 115 each. The rf power was 400 W. The etch rate was 40 Å/s and etching was continued for 28 s for partial removal of the cap layer (approximately 1100). On the other hand, wet etching was carried out in a solution of 25 mg KOH, 1 mg $K_2Cr_2O_7$, 25 ml propanol in 100 ml of water at 26 °C. The etch rate was 160 Å/min and etching was continued for 7 min. Both the dry and wet etched samples were annealed at temperatures of 500, 600, 700, and 800 °C for 60 s in a rapid thermal process (RTP) reactor under vacuum. SiO_2 was then deposited by low-pressure CVD at 450 °C. The thickness of SiO_2 was 400 Å. Al dots were then evaporated through a metal mask by thermal evaporation to make metal–oxide–semiconductor (MOS) capacitors. Back contact was made with Al deposition on the Si substrate. A postmetal annealing was carried out at 350 °C in N_2 ambient. A completed sample is shown in Fig. 1. High-frequency $C-V$ measurements were performed using 4145B semiconductor parameter analyzer and a Boonton 71BD capacitance meter.

Figure 2(a) shows a typical $C-V$ profile obtained for the wet etched samples. The presence of a distinct kink in the unannealed sample in Fig. 2(a) indicates that the SiGe layer is coherently strained. However, the nature of the kink changed as the annealing was performed at temperatures of

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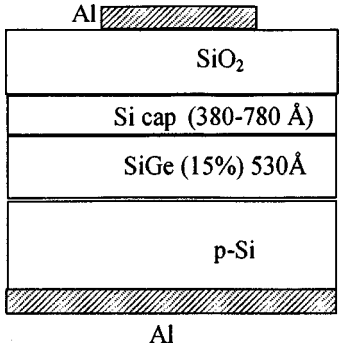

FIG. 1. Schematic drawing of the MOS device structure used for investigation.

500, 600, and 700 °C. No such kink was observed for samples annealed at 800 °C. On the other hand, as shown from the $C-V$ plots obtained for the dry etched sample [Fig. 2(b)], a kink is observed for the unannealed sample. As the sample is annealed at 500 and 600 °C, the shape of the kink changes before it disappears with higher annealing temperatures. A comparison of Figs. 2(a) and 2(b) indicates that the kinks obtained for the dry etched 500 and 600 °C samples are similar to the ones obtained for the wet etched sample annealed at 600 and 700 °C, respectively.

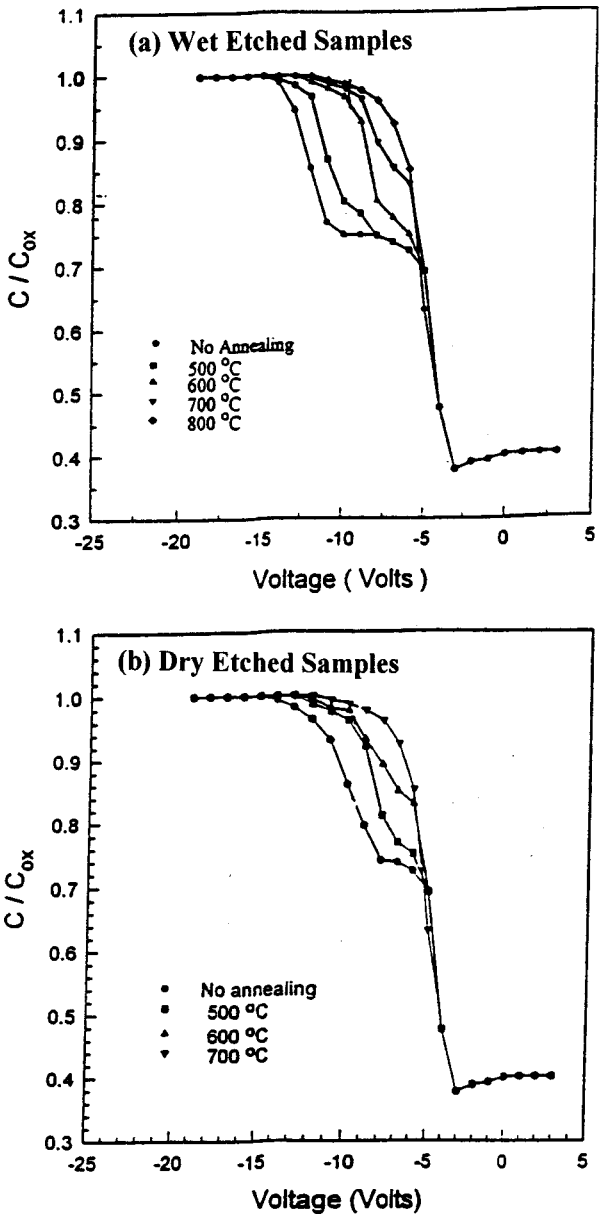

FIG. 2. $C-V$ plot obtained for the wet etched samples (a) and dry etched samples (b) annealed at different temperatures.

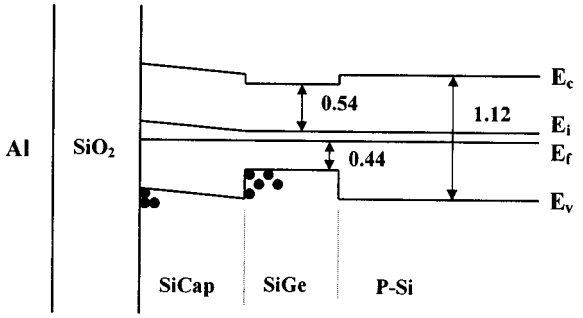

FIG. 3. Hole confinement in the quantum well leading to the kink in the $C-V$ measurements.

To explain the appearance of such kinks a simple model is proposed. When the MOS device is driven into accumulation from inversion, the substrate being p-type Si, holes are attracted from the bulk towards the interface, under the action of increased negative voltage. In the absence of the strained SiGe layer the holes are expected to accumulate uninterruptedly at the oxide/Si cap interface. Under such a condition, a continuous increase in capacitance is expected until it reaches a constant maximum value equal to C_{ox}. However, in the presence of a strained SiGe layer, as in our case, some holes on their way towards the oxide/Si interface are trapped within the quantum well (QW) as a consequence of band-gap narrowing due to coherent strain. As shown in Fig. 3, hole confinement results in a decrease in the total capacitance because of the series combination of C_{ox} and $C_{\mathrm{SiGe\,QW}}$. The capacitance of the cap layer is neglected as the device was driven into accumulation. When the applied voltage becomes more negative, such that the holes confined inside the quantum well are negligibly small compared to holes accumulated at the oxide/Si interface, the capacitance increases and finally equals C_{ox}. This mechanism results in the appearance of a distinct kink for the wet etched unannealed sample. However, as the sample is annealed at 500, 600, and 700 °C, the coherent strain in the SiGe layer is reduced, and hence, the band-gap narrowing effect also decreases. This spreading of the band gap results in a decrease in the well height (amount of discontinuity in the valence-band edge: ΔE_V). Hence, the number of holes captured in the well decreases, thus allowing a larger number of holes to accumulate at the oxide/Si interface for the same applied potential. This mechanism results in an increase of capacitance for the samples annealed at a higher temperature as compared to their low-temperature counterparts. Samples annealed at 800 °C show no such kink, indicating the absence of the hole capture mechanism. This clearly indicates that the coherent strain in SiGe is lost, resulting in complete relaxation of the SiGe layer. The appearance of kinks for the dry etched samples can also be explained by a similar mechanism. However, the kink for the unannealed dry etched sample shows a reduced number of holes in the quantum well, indicating partial relaxation.

A numerical estimate of the band gap for the plasma as well as wet etched samples annealed at different temperatures can be made by making use of the hole density of state

TABLE I. Value of $(1-[C/C_{ox}])$ and the calculated band gap in eV for the dry as well as wet etched samples after being annealed at different temperatures.

		No annealing	500 °C	600 °C	700 °C	800 °C
$(1-[C/C_{ox}])$	Wet	0.2375	0.1875	0.0625	0.0187	0
	Dry	0.13125	0.05	0.016	0	0
Calculated band gap (eV)	Wet	1.013	1.019	1.048	1.079	1.10
	Dry	1.034	1.054	1.083	1.10	1.10

in the valance band. The number of holes captured in the quantum well is directly related to the valance-band discontinuity occurring due to coherent strain in the SiGe film. It is well known that the number of holes near the valance band is given by[9]

$$p = N_v \exp[-(E_f - E_v)/kT]/\mathrm{cm}^3, \tag{1}$$

where

$$N_V = 2[2m_{dh}kT/h^2]^{3/2}/\mathrm{cm}^3, \tag{2}$$

where, m_{dh} = hole effective mass. Wang *et al.*[10] have reported a value of 0.44 mo for the hole effective mass for their sample ($Si/Si_{0.85}Ge_{0.15}/Si$), which is identical to ours. In this case, the valance-band maximum of $Si_{0.85}Ge_{0.15}$ is ~75 meV lower than that of Si, assuming $\Delta E_v \gg \Delta E_c$.[10] Substituting the value of m_{dh} in Eq. (2) we get $N_v = 3.654 \times 10^{24}\,\mathrm{cm}^{-3}$. The number of holes captured inside the quantum well can be calculated from the $C-V$ curve (Fig. 2) by the following method. Values of $\{1-(C/C_{ox})\}$ at a given applied bias for samples (dry as well as wet etched and subsequently annealed) are summarized in Table I.

The value of C_{ox}, calculated using the simple formula $(k\epsilon_0 A/d)$, where A = area of the MOS device (diameter: 300 μm), k = dielectric constant for the oxide (3.9), and d = thickness of the SiO_2 layer (400 Å) is 61 pF. Using the value of C_{ox}, $C_{SiGe\,QW}$ can be calculated for all the samples. Multiplying C with the applied bias, V (10 V), the total charge (Q) can be estimated. Dividing Q by the electronic charge would give the number of holes trapped in the quantum well, which will allow us to compute the hole density p/cm^3. The value of ''p,'' thus calculated, for the wet etched, unannealed sample is $0.2036\times10^{18}/\mathrm{cm}^3$ (for $C_{SiGe\,QW} = 195\times10^{-12}$ F). Substituting ''p'' in Eq. (1), we obtain

$$3.654\times10^{24}\exp[-(E_f-E_v)/kT] = 0.2036\times10^{18}/\mathrm{cm}^3. \tag{3}$$

Simplifying Eq. (3) gives

$$(E_f - E_v) = 0.434 \text{ eV}. \tag{4}$$

Using similar methodology, the (E_f-E_v) values were computed for all the samples. It is known that the band discontinuity for strained SiGe occurring at the conduction band is much smaller as compared to the valance band and has a value of 0.02 eV. So, (E_c-E_i) has a value of $[(1.12/2) - 0.02] = 0.54$ eV, for the strained SiGe film, where 1.12 eV is the band gap of Si. The band gap (E_c-E_v) can be expressed by the following:

$$(E_c-E_v) = (E_c-E_i)+(E_i-E_f)+(E_f-E_v) \text{ eV}. \tag{5}$$

Substituting the value of (E_f-E_v), in Eq. (5), the band gap for the samples can be calculated and is summarized in Table I.

Since wet etching is known to be a nondestructive technique, the wet etched unannealed samples would be coherently strained. Hence, the band gap of such samples would be less than the silicon band gap by a factor of $(\Delta E_v + \Delta E_c)$. As seen from Table I, the band gap for the wet etched unannealed sample is 1.013 eV. Also, ΔE_v and ΔE_c have values of 0.075 and 0.020 eV,[10] which are in agreement with the silicon band gap. It may also be seen from Table I that the band gap increases progressively to 1.10 eV with increase in annealing temperature to 800 °C. This indicates that the coherent strain in the SiGe layer is becoming relaxed with the increase in annealing temperature and a complete relaxation takes place at 800 °C. The relaxation of the samples annealed at 500, 600, and 700 °C can be considered to be predominantly due to the creation of dislocation loops due to RIE and their subsequent annealing. As the SiGe samples were grown at 700 °C, these samples when annealed at 800 °C will have dislocation loops induced causing relaxation. Also, plasma etching of these samples will enhance the relaxation mechanism. On the other hand, a comparison of band-gap values for the dry and wet etched samples annealed at a given temperature indicate a higher value for the dry etched samples. This indicates an advanced relaxation mechanism in the dry etched samples. Also, as may be seen from Table I, the dry etched, 700 °C annealed sample has a band gap of 1.10 eV, indicating a complete strain relaxation takes place at a lower temperature as opposed to 800 °C for the wet etched samples.

In conclusion, the effect of plasma etching and subsequent annealing on the valence-band discontinuity E_V at the Si/SiGe interface was studied. Dry etched samples demonstrated a faster relaxation mechanism as compared to their wet etched counterparts. In both dry and wet etched samples as the annealing temperature increases the valence-band discontinuity is reduced and completely disappeared at higher temperature annealing. A simple technique is proposed to measure the band gap of the SiGe films by a $C-V$ measurement using a MOS structure.

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